

German Verification Day

March 4, 2005

Carl von Ossietzky University Oldenburg, Germany

The two German top projects on verification and analysis of embedded systems, the DFG funded long-term research project AVACS, a Transregional Collaborative Research Center (SFB/TR), and the BMBF funded applied research project VERISOFT, are presenting selected results from their first year of research, within the first German Verification Day, on March 4, 2005, at the Carl von Ossietzky Universität Oldenburg. Whereas AVACS' research challenge is of foundational nature, developing novel verification algorithms covering the design space of complex embedded systems, Verisoft's challenge is to achieve fully verified components for industry-critical systems, employing state-of-art automatic and interactive verification tools.

The foundational project AVACS (www.avacs.org) combines the expertise in formal verification at its three sites Freiburg, Oldenburg, and Saarbrücken to address the rigorous mathematical analysis of models of complex safety critical computerized systems, such as aircrafts, trains, cars, or other artifacts, whose failure can endanger human life. AVACS aims at raising the state of the art in automatic verification and analysis techniques of such complex systems from its current level of applicability to isolated points in the design space of such systems to a level allowing a comprehensive, holistic, and ultimately automatic verification of such systems, with research activities structured into three key project areas, addressing verification of real-time systems, hybrid systems, and holistic system verification, respectively. New results presented will include novel techniques in the verification of hybrid and real-time systems.

The VERISOFT project (www.verisoft.de) combines the expertise of key industrial (BMW, Infineon, T-Systems) and academic teams to achieve fully verified key application components, covering the full design layer from applications to hardware, strengthening the competitive positioning in the addressed industrial sectors by being able to offer fully formally verified components. To this end, formal mathematical proofs will be rigorously established using a combination of state-of-the-art interactive and automatic verification methods. Presentations will report significant progress on the complete formal verification of an industrial embedded processor, of a compiler for a large subset of C and of an operating system.

For the Program of the German Verification Day, see attachment. More information about this event can be found at www.avacs.org/gvd. Registration starts at December 13, 2004 and ends at January 31, 2005.

Werner Damm

Carl von Ossietzky Universität Oldenburg

Wolfgang Paul

Universität des Saarlandes

Co-Organizers

German Verification Day Workshop Program

Thursday, March 03, 2005

- 19:30 *Welcome*
Dr. Pantel, Stadt Oldenburg
- Reception and Pre-Event Dinner* at the Horst-Janssen Museum, Oldenburg

Friday, March 04, 2005

- 09:00-09:30 *Welcome*
- Prof. Dr. Uwe Schneidewind, President of the Carl von Ossietzky Universität Oldenburg
 - Dr. Reuse, BMBF
 - Dr. Sonntag, DFG
 - Prof. Dr. Werner Damm, Scientific Director SFB/TR 14 AVACS
 - Prof. Dr. Wolfgang Paul, Scientific Manager VERISOFT
- 09:30-09:45 *The SFB-Transregio AVACS - A Survey*
Werner Damm, C.v.O. Universität Oldenburg
- 09:45-11:45 *Selected Presentations from AVACS*
- 11:45-12:30 **Invited Presentation**
Recent Developments in real-time verification: what's up with UPAAL
Kim Larsen, Aalborg University
- 12:30-13:30 *Lunch*
- 13:30-14:15 **Invited Presentation**
Formal Verification in the Airbus System Development process
Francois Pilarski, Airbus Industries, F
- 14:15-14:30 *The BMBF project VERISOFT – A Survey*
Wolfgang Paul, Universität des Saarlandes
- 14:30-16:30 *Selected Presentations from VERISOFT*
- 16:30 *Closing*